IN THE SPECIFICATION:

Replace the paragraph bridging pages 1 and 2 with the following:

The design of a semiconductor integrated circuit is divided roughly into two of a circuit design and a layout design. When the circuit design is carried out, the description of functions corresponding to the specs of the semiconductor integrated circuit and a logic combining constraint file based on timing specs is created. A logic combinable RTL (Register Transfer Level), which is one of abstract levels where hardware is described in language, has been widely used in the description of the functions corresponding to the circuit specs. The created constrained file includes an ideal clock cycle, a clock delay, a skew, etc. Here, the clock delay means a delay from an input port to, for example, each of flip-flop circuits.

Replace the entire paragraph on page 29 with the following paragraph:

The present invention provides an apparatus for designing a semiconductor integrated circuit, which is capable of satisfying timing constraints without providing BFBs, and improving a convergent property at optimization, and a design method therefore. An LSI automatic design simulator (10) determines the number of clocks employed in a clock generating functional part (30) and delays in respective clocks, allocates the clocks set as clock systems, and verifies constraint conditions with respect to design, based on the respective clocks. A tree determining functional part (32) adjusts skews of the respective clocks through the use of the produced clock systems, makes delay adjustments to the clocks, verifies a layout adjustment, and fetches therein data supplied thereto without time constraint violation, thereby making it possible to further enhance a convergent property that satisfies all of timing constraints.